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Japanese Laid-Open Patent

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Inventor: Shunpei Yamazaki

Applicant: Semiconductor Energy Laboratory

SPECIFICATION

1. Title of the Invention

INSULATED GATE FIELD EFFECT SEMICONDUCTOR DEVICE

2. Scope of Claims

1. An insulated gate field effect semiconductor device, characterized in that a channel forming region is formed under a gate in a semi-amorphous semiconductor formed on a substrate and having a microcrystalline property.

2. An insulated gate field effect semiconductor device, characterized in that a pair of impurity regions are formed, on a semi-amorphous semiconductor having a microcrystalline property on a substrate, while sandwiching a channel forming region therebetween, and that a gate electrode is formed on said channel forming region and an insulating material.

3. An insulated gate field effect semiconductor device according to claim 2, characterized in that a field insulating material is formed on the pair of impurity regions forming a

source and a drain.

3. Detailed Description of the Invention

The present invention relates to an insulated gate field effect semiconductor device (hereinafter called IGFET) and particularly relates to an IGFET for obtaining characteristics similar to those of a single crystal semiconductor even in a thin film type structure by using a semi-amorphous semiconductor (hereafter called SAS) formed on a substrate and having a size of from 5 to 200 Å and a microcrystalline property in a channel forming region under a gate.

In the present invention, the SAS is formed by a plasma CVD method on the substrate, particularly, a substrate causing no reaction on a semiconductor on an upper face of this substrate, e.g., a glass or ceramic substrate and a conductive substrate in ohmic contact, and is positively used in the IGFET. This SAS is described in a Japanese Patent Application (semi-amorphous semiconductor in Japanese Patent Application No. Sho 56-065826, filed in April 30, 1981, and Japanese Patent Application No. Sho 55-120322, filed in August 30, 1980) filed by this inventor.

Namely, the inventor of the present invention has experimentally found that when optical energy of AM1 (100 mW/cm^2) in electricity-light conductivity is given to a

substrate, particularly, a glass substrate of an amorphous structure, having no single crystal in a semiconductor, e.g., a silicon semiconductor, and a stainless substrate of a single crystal structure, a value from $1x10^{-3}$ to $8x10^{-2}$ $(\Omega cm)^{-1}$ is obtained and is 1/2 to 1/10 in comparison with the single crystal silicon semiconductor and provides very excellent characteristics.

In the present invention, such characteristics of the SAS are used in the IGFET.

Further, the present invention is based on the fact that there are no characteristics of the original SAS and no satisfactory characteristics are obtained when such a SAS is applied to the IGFET of a thin film type conventionally known, i.e. a longitudinal sectional structure shown in Fig. 1.

Namely, a structure shown by a longitudinal sectional view of Fig. 1 is known as an IGFET using a conventional amorphous semiconductor (called AS). In Fig. 1, gate electrodes (3) and (13) are formed by a heat-resistant material such as molybdenum on an insulating substrate (1). Further, a gate insulating film (11) is formed by silicon oxide having a thickness of from 0.1 to 0.5 μm by a CVD method. Next, an AS is formed on an upper face of this gate insulating film (11) by selective etching only on channel type gates (5) and (10). Further, semiconductor layers (6) and (7) of an N-

type in an N-channel IGFET (12) are selectively formed by using a photoetching method. With respect to a P-channel type IGFET (2), aluminum is formed by a vacuum evaporation method and a source (9) and a drain (8) are made by selective etching so that a C/MOS · FET is completed as shown in Fig. 1.

In this structure, since the gate insulating material (11) is formed by the CVD method, density is not high so that the gate electrode (3) and the semiconductor (5) are easily short-circuited. Therefore, the insulating material (11) must be set to a thick thickness equal to or greater than 0.3 μm. As a result, a gate voltage becomes a high voltage from 20 to 60 V so that no so-called low voltage driving operation of from 1.5 to 5 V can be performed.

Further, it is necessary to precisely align both ends of the gate electrode (15), both ends of the semiconductor (5) and one ends of the source (6) and the drain (7). However, it is impossible to perform the aligning operation with high accuracy of 1 μm or more in an irregular state on the substrate. As a result, a tolerance of 20 to 30 μm is made so that a drain voltage also becomes a high voltage of from 50 to 70 V and no low voltage driving operation of from 1.5 to 10 V can be performed. Further, a semiconductor having a large quantity of doped impurities of a P or N conductivity type from 0.5 to 2% comes in close contact with a surface (17) of

the semiconductor (5) coming in contact with a so-called channel forming region having a structural sensitive property. The source (6) and the drain (7) are short-circuited in this close contact portion unless these impurities are perfectly removed by etching. However, since these impurities have the same principal component as the semiconductor (5) beneath them, it is extremely difficult to perform the selective etching.

Further, in the structure of Fig. 1 having a completed rear face, the semiconductor, mainly, the SAS having the structural sensitive property is not reliable at all and cannot be practically used in industry due to dispersion in manufacture since this structure is exposed to the air. When such a structure is used, the structural sensitive property of the semiconductor may not become a serious problem in the AS. However, in the case of Fig. 1, such a structure is not suitable for the SAS.

The present invention is characterized in that the SAS is used in the channel forming region and all of lower, upper and side portions are covered with a semiconductor having an insulating material or a high impurity concentration, and the operation of a gate is controlled by utilizing the structural sensitive property of this semiconductor. Therefore, the present invention is also characterized in that a driving operation can be performed by using each of a gate voltage and

a drain voltage of from 5 to 10 V instead of a conventional voltage of from 40 to 80 V, and further can be essentially performed by using a voltage of 1.5 V in this structure.

In Fig. 1, the semiconductor device is made by using a photomask four times, but the gate electrode (4), the source (6) and the drain (7) are constructed by materials of different kinds. When a lead wiring is made of a metal of small resistance on the substrate, the photomask is further required twice on an upper surface of this substrate. Accordingly, the photomask is required six times in total, but only a single layered wiring is formed.

The present invention removes the defects explained above and is mainly characterized in that the semiconductor device is easily integrated and a resistor and a capacitor as other important elements are simultaneously integrated and are easily made in addition to a channel forming region formed by the SAS.

The embodiments of the present invention will next be explained with reference to the drawings.

Embodiment 1

Fig. 2 is a longitudinal sectional view showing a manufacturing process of an IGFET of the present invention.

In Fig. 2(A), a SAS (20) having a thickness of 0.1 to 1 μm is formed by a plasma vapor phase method on glass as a

translucent substrate having an insulating property on the side of a substrate (1), or stainless steel as a conductive substrate. In this SAS, silane (monosilane or polysilane) or silicon fluoride is diluted with helium or hydrogen, and is guided into a reaction furnace of 0.01 to 10 torr such as 0.3 torr. Then, electromagnetic energy of a direct current, a high frequency (500 KHz to 50 MHz, e.g., 13.56 MHz) or a microwave (1 to 10 GHz, e.g., 2.45 GHz) is applied to the above reactive gas on the substrate heated to a temperature from 100 to 400°C, e.g., 300°C with an output of from 20 to 200 W so that glow discharge or arc discharge is caused. Thus, the reactive gas and a carrier gas are formed as plasma and are decomposed and reacted. Thus, the SAS of a true property or a substantially true property having a microcrystalline property is formed on the substrate.

This SAS has a crystal property having the size of a short range order from 5 to 200 Å, and 0.01 to 5 mol% of the SAS is added to a recombination central neutralizer using hydrogen for neutralizing dangling bonds of silicon and a halogen element such as fluorine. Further, an alkali metal such as lithium, sodium or potassium may be also added at a concentration of from 10^{14} to 10^{17} cm^{-3} to neutralize the dangling bonds canceled by these neutralizers of this SAS at a concentration of from 10^{13} to 10^{15} cm^{-3}.

This SAS has $1x10^{-5}$ to $3x10^{-3}$ $(\Omega cm)^{-1}$ in dark conductivity, and is large by 10^2 to 10^4 times in comparison with AS having 10^{-7} to 10^{-6} $(\Omega cm)^{-1}$. Optical conductivity experimentally ranges from $1x10^{-3}$ to $8x10^2$ $(\Omega cm)^{-1}$ under a condition of AM1 and is particularly large by 10 to 10^3 times in comparison with AS having 10^{-6} to $3x10^{-4}$ $(\Omega cm)^{-1}$.

Therefore, mobility of each of an electron and a hole flowing through this SAS is larger by 10^2 to 10^4 times than the AS. Accordingly, it is very important to use this SAS as a semiconductor for the channel forming region of the IGFET on making the semiconductor device for a high speed response.

Further, as shown in Fig. 2(A), a mask (21) having a thickness of from 1 to 5 μm is selectively formed and a first mask ① is used here. This mask may be formed by a polyimide film and a PIQ as silicon oxide or heat-resistant organic resin by a reduced pressure plasma vapor phase method.

In Fig. 2, a source region (26), a drain region (27) and a channel forming region (24) are formed in a region (22) of the IGFET.

Thereafter, a semiconductor layer (25) of AS or SAS having a thickness of from 0.1 t 1 μm is again formed on an upper face of this region (22) by a method similar to that in the semiconductor layer (20). At this time, 0.2 to 2% of phosphorous as impurity of V-valence and boron as impurity of

III-valance is added to each semiconductor layer of an N or P type to make the IGFET of an N or P channel. Thus, the obtained material is shown in Fig. 1(A).

In Fig. 2(B), the mask (21) is dipped into an etching liquid with a ultrasonic wave to slightly applied to this mask in the structure of Fig. 1(A) and is dissolved and removed. Thus, semiconductor layers (29) and (30) of one conductivity type constituting a pair are formed as a source and a drain in the regions (26) and (27). Further, a field insulating material (31) having a thickness of from 0.1 to 1 μm is formed on upper faces of these layers by a film of silicon oxide or polyimide resin as shown in Fig. 2.

Next, a portion corresponding to the region (24) and the field insulating material of an opening hole (32) for contact with an electrode are selectively removed by a second photomask ②.

Thereafter, a gate insulating material (33) having a thickness from 300 to 2000 Å is formed by a plasma oxidizing method. Namely, oxygen or an oxidizing gas is decomposed and activated by a microwave of 2.45 GHz (an output of 100 to 500 W), and the substrate is arranged within this activated oxidizing gas at a temperature of from 300 to 500°C. Then, an oxide, particularly, a silicon oxide film is formed on this substrate surface when the SAS (20) is constructed by silicon.

A nitriding gas such as ammonia, etc. may be used instead of the oxidizing gas. An insulating film of silicon oxide, silicon nitride, etc. having a thickness of from 300 to 2000 Å may be also formed by the plasma vapor method. Further, when a non-volatile memory is formed, it is effective that a semiconductor or a lump-shaped cluster or a thin film of a metal within this gate insulating material and is set as a charge capturing center. Further, an MNOS structure may be also formed. In the present invention, these structures have a degree of freedom determined by application of this IGFET.

Thus, after the gate insulating material (33) is formed, an opening (32) is formed in the source or the drain (the drain in Fig. 2) by a third photomask ③. Thereafter, electrodes (35), (34) and a lead wire (36) are formed by a metallic film by selectively using a fourth photomask.

These electrodes and the lead wire are effectively manufactured by using a method using a vacuum evaporation method of aluminum, etc. and a photoetching method, or an electroless plating method of a metal such as nickel, etc. and the photoetching method.

In view of reliability, it is preferable to use a combination method of a lift-off method and the electroless plating method such that the insulating film or the semiconductor layer on a lower side of these metals is not

impregnated with these metals. Namely, in Fig. 2(D), similar to Fig. 2(A), a resist for a mask is formed in portions where the electrode lead wires (35) and (36) are not formed, and a metallic film is formed on an upper face of this resist and the other one face. Thereafter, only the mask and the metallic film on this mask are selectively dissolved and removed.

Thus, an IGFET having the structure shown in the longitudinal sectional view of Fig. 2(D) is obtained. At this time, a pair of impurity regions (29) and (30) functions as a source and a drain, and a channel forming region (19) having a channel length of from 0.3 to 20 μm, particularly, from 2 to 3 μm can be formed. Accordingly, it is possible to obtain a high frequency response by 10^3 to 10^6 times in comparison with the structure of Fig. 1 using the conventional AS. Further, a driving voltage can be set to range from 1.5 to 10 V and typically range from 5 to 10 V so that the driving voltage can be reduced by 1/2 to 1/5 times in comparison with the conventional case. As can be clearly seen from the drawings, an upper side of the SAS constituting the channel forming region (19) is covered with the gate insulating material (33) and this SAS is formed on the thin substrate (1) having a lower side electrode. All of upper, lower and side faces of the channel forming region are particularly covered with the insulating film and the semiconductor so that no channel

forming region is deteriorated in contact with the atmosphere.

In the present invention, the SAS has an extremely high structural sensitive property in comparison with the AS. A certain convex portion, particularly, a metallic electrode is not arranged on the substrate, but this SAS is formed on a material unreacting on the SAS such as a flat glass substrate, etc. The semiconductor layer (25) adding impurities thereto is laminated and formed on the channel forming region of this SAS. Accordingly, no problem exists in that these impurities are doped and leak is caused, etc. Theses are the characteristics of the present invention.

In the present invention, only one IGFET is shown, but plural IGFETs are easily integrated and formed on the same substrate. Further, it is also easy to form an interlayer insulating material on the lead wire (36) and arrange a second lead wire in multilayer arrangement.

When the substrate (1) is constructed by translucent glass, the substrate can be operated as a phototransistor for irradiating light from a lower layer and detecting an existence degree of this light. Further, it is also possible to make various kinds of applications in which this substrate can be integrated and used as a semiconductor device for imaging, etc.

The present invention has been described with silicon as

a center. However, SiO_x ($0<x<1$), Si_3N_{4-x} ($0<x<4$), germanium and III-V compound may be also used.

4. Brief Description of the Drawings

Fig. 1 is a longitudinal sectional view of a conventional semiconductor device.

Fig. 2 is a longitudinal sectional view showing a semiconductor of the present invention and a manufacturing process thereof.